A COMPLETE SINGLE CHIP AM/FM RADIO INTEGRATED CIRCUIT

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1. Abstract

We have developed a complete single chip AM/FM radio integrated circuit embodying all the necessary function for an AM/FM radio system. It includes the AM/FM front end, AM/FM IF amplifiers, AM AGC, AM/FM detector, audio pre and power amplifiers, variable capacitor diode for the FM AFC, tuning indicator circuit, electric volume, as well as a regulated supply. As a result, the application of this IC enables a complete AM/FM radio system without any use of active components.

The static current consumption of the AM and FM are 3 mA and 5 mA, respectively, including the audio stage, while the operating voltage ranges from 1.8 V to 9 V. This low power consuming and low voltage operating IC integrates approximately 700 elements on a 2.4 mm x 3.1 mm chip.

2. Introduction

The development of the single chip radio IC has advanced from a block IC for individual function to a system IC including from IF stage to the audio stage. However, the block of FM front end, including the audio stage, has not been integrated on a single chip up to the present for the following reasons:

(1) A monolithic IC process must satisfy certain conditions in order to enable integration from front end handling VHF band to the audio final stage on a single chip; a sufficiently high frequency and noise characteristics must be obtained with a low saturation voltage of the power transistor at a large current.

(2) Integrating on a single chip FM receivers having a total gain as large as 140 dB causes instability and beat interference.

(3) The heat from the power amplifier causes instability and thermal interference of the FM front end.

The newly developed IC has cleared the above problems by effectively applying the new circuit technology and developing the high frequency IC process. This paper reports on the detail of the IC.

3. Design Consideration

In designing this IC, we have focused on the following standards. The IC should:

(1) have all the necessary function for an AM/FM radio while using a considerably small chip.

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(2) be with high sensitivity and stability.

(3) reduce the number of external components and adjustments as much as possible.

(4) have a large audio power output.

(5) have a low power consumption as well as operate at a low voltage.

Items (1) and (3) aim at the reduction and simplification of the assembly process and at the effective application of the IC to a super micro radio. Items (2) and (4) will satisfy almost all radio categories, while Item (5) enables stable operation by dropping the higher harmonics power which causes instability and beat interference, as well as aims at being useful in the field of battery-operated radios.

4. Circuit Description

Figure 1 shows the block diagram of the IC. The followings are the detail description of each block:

FM FRONT END

The FM front end consists of a RF-amplifier, a mixer, a local oscillator, a buffer amplifier for the local oscillator, and a post IF amplifier. Figure 2 shows the circuit diagram.

RF amplifier Q1 is a base-grounded amplifier with a low noise transistor, where the NF and PG are 3 dB and 12 dB, respectively, at 100 MHz.

The mixer is a double-balanced mixer consisting of Q2 - Q7, which prevents the leakage of the local oscillator signal as well as the RF input signal at the mixer output, enabling an effective common mode rejection.

The local oscillator consists of the differential pair, Q14 and Q15, and is of a positive feedback type. Local oscillator frequency drift is caused by three factors, namely, (A) power source voltage fluctuation, (B) ambient temperature fluctuation, and (C) pellet temperature fluctuation, and each drift is compensated for by the following methods:

(A) is solved by the voltage regulator in the IC which outputs a stabilized DC voltage of from 1.8 V to 9 V.

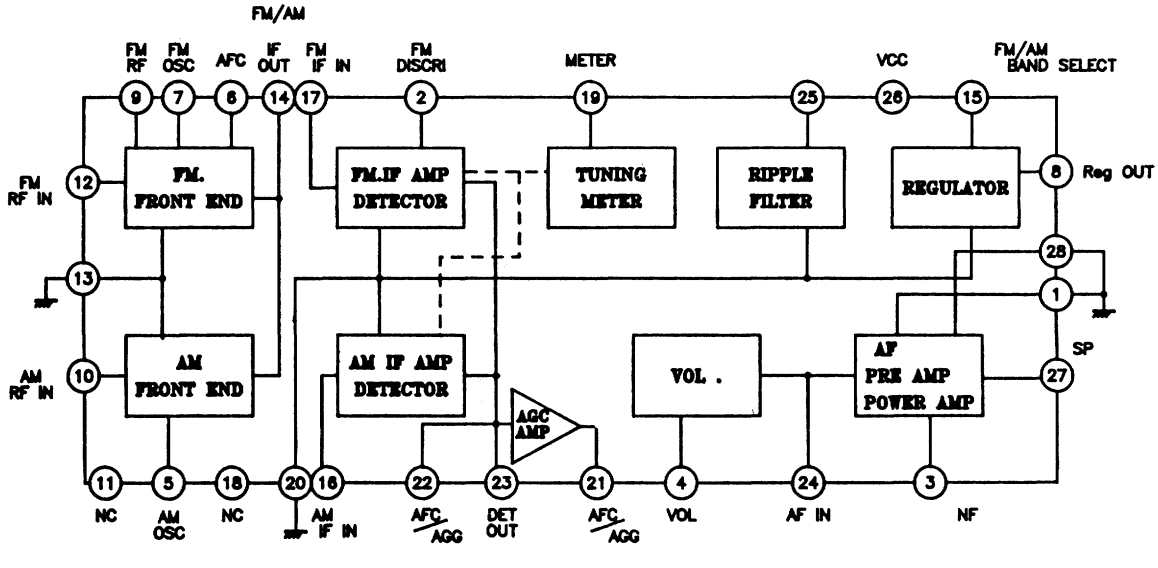


Figure 1: Block Diagram of the IC

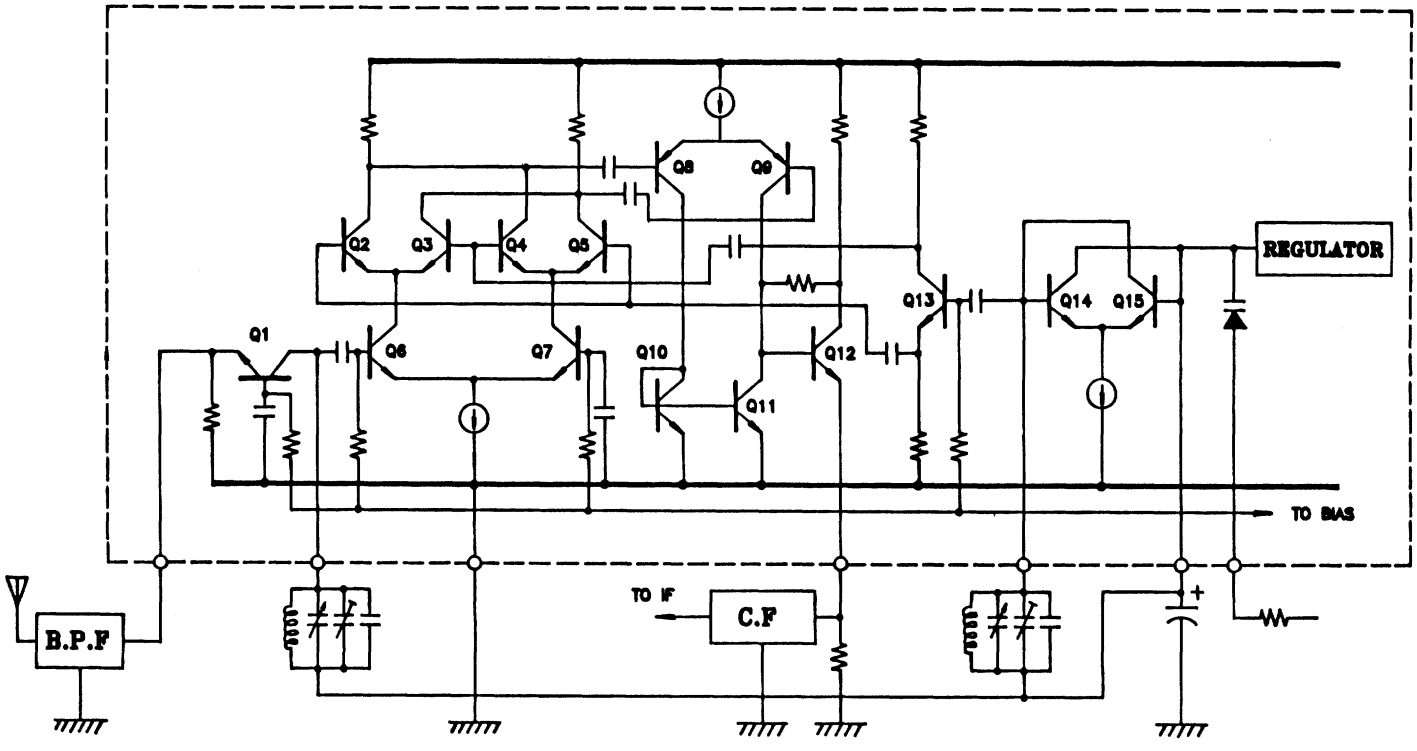


Figure 2: Circuit Diagram of the FM Front End

Figure 3 shows the frequency drift to the power source voltage.

As for (B), the frequency drift is reduced by using a negative coefficient capacitor in the resonant circuit, as oppose to the junction capacitor in the transistor which has a positive thermal coefficient. The drift is also reduced by keeping the bias current of the differential pair, Q14 and Q15, constant.

As the IC embodies the power amplifier, the pellet temperature rises independently of the ambient temperature, and thus, the capacitor in the resonant circuit does not compensate for the frequency drift. Thus, as for (C), the frequency drift is reduced by using a low parasitic capacitor in the transistors and using a bias voltage with a temperature coefficient. The bias voltage decreases with the temperature rise, and consequently, this frequency drift is reduced to within -30~-50 kHz at 110.7 MHz with a constant output power of 500 mW. The drift is negligibly small as the output power for practical use is only scores of mW. Figure 4 shows the drift to the power output. The drifts of (B) and (C) do not contradict with each

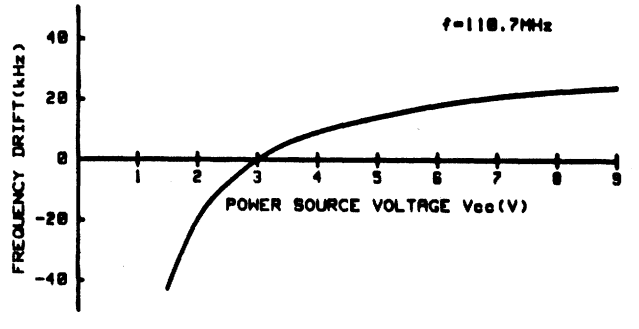


Figure 3: Frequency Drift of the Local Oscillator to the Power Source

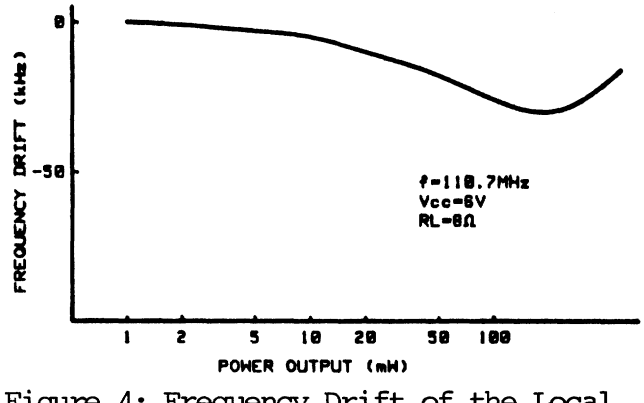


Figure 4: Frequency Drift of the Local Oscillator to the Power Output

other, as they may be compensated for by the same method.

The local oscillator is reduced to as low as 600 mVp-p to control its leakage to other circuits and to reduce radiation. With this IC, the local oscillator circuit is surrounded by N^+ type diffusion island which is located under the resistor of the local oscillator circuit, and is connected to the regulator bias voltage. It is thus isolated from the other circuits, and effectively reduces the junction capacitor fluctuation caused by the power source voltage change.

The buffer amplifier Q13 protects the local oscillator from a large RF input signal, and supplies the differential output of the local oscillator to the double-balanced mixer.

Post IF amplifier, consisting of Q8 - Q11, is constructed with a differential amplifier and a current mirror circuit, and provides an effective common mode rejection without being influenced by the Vcc line or the ground line. The output transistor Q12 is a single-ended emitter follower and is connected to the IF filter.

The conversion total gain of the FM front end is 40 dB while the NF is 5 dB.

FM IF AND DETECTOR

The FM IF amplifier is constructed by a seven-stage differential amplifier, and operates as a capacitor coupling amplifier for a low voltage operation with a band pass characteristics with a center frequency of 10.7 MHz. Compared with the direct coupling amplifier, the capacitor coupling amplifier does not transmit low frequency noise and interference signal from the IF input terminal, and therefore, is more advantageous. It also requires no negative feedback to stabilize the operating bias. Figure 5 shows the IF gain to the frequency.

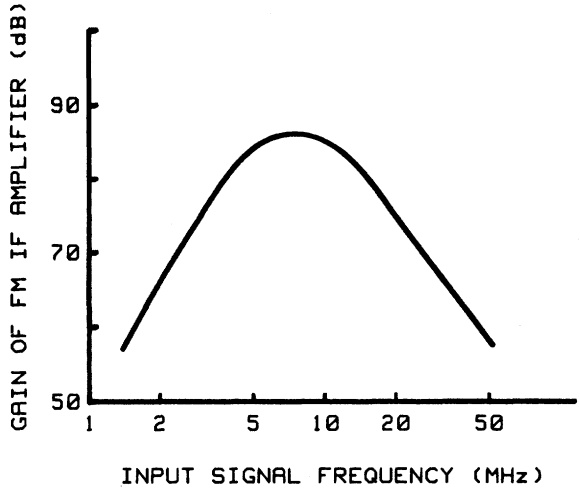


Figure 5: Gain of the IF Amplifier to the Input Signal Frequency

The FM detector uses a low distortion quadrature detector circuit and a circuit consisting of a differential amplifier and a ceramic resonator at the phase shift stage. Figure 6 shows the circuit diagram.

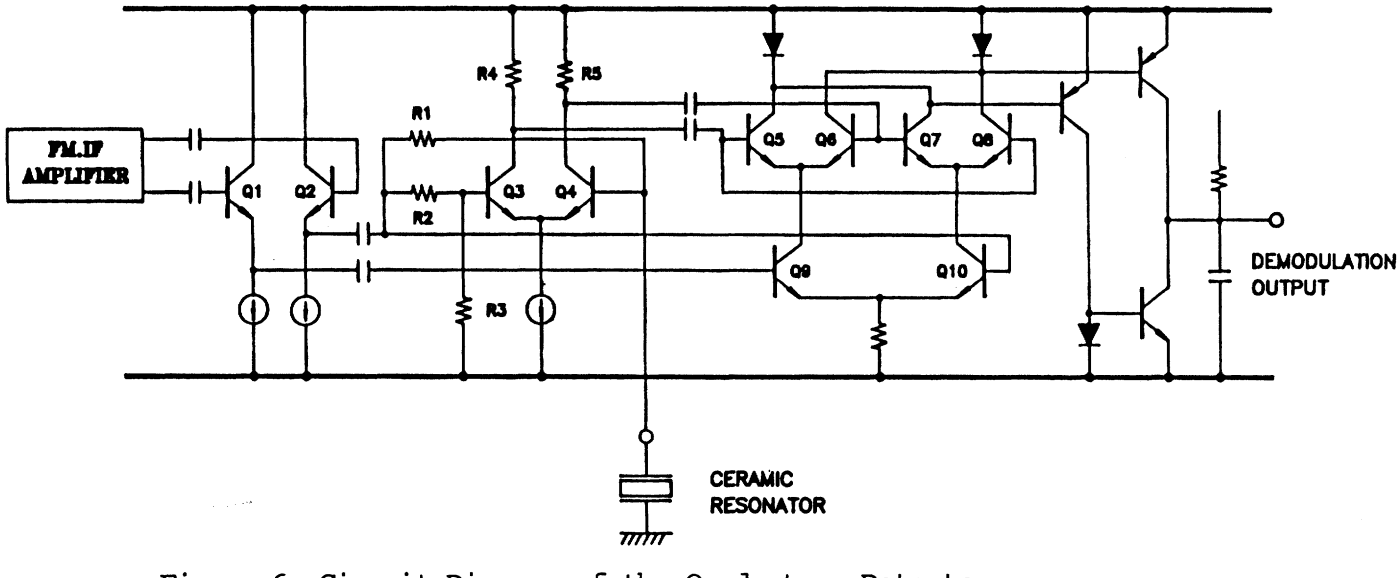


Figure 6: Circuit Diagram of the Quadrature Detector

The system operation is carried out as follows: First of all, the IF limitter signal amplified by the seven-stage IF amplifier is taken out by the emitter follower amplifiers, Q1 and Q2, and is then input into a differential amplifier by passing through the bridge circuit consisting of R1, R2, R3, and a ceramic resonator used for this IC, as shown in Figure 7, operates similarly to an inductor, within a band with a center frequency of 10.7 MHz. The operation of the phase shift stage is explained according to Figure 8.

The base input signals of Q3 and Q4 are expressed by the below equations where L is an equivalent impedance of the ceramic resonator:

$$V_A = \frac{R_2 \cdot V_{IN}}{R_2 + R_3} \quad (1)$$

$$V_B = \frac{j_{WL} \cdot V_{IN}}{R_1 + j_{WL}} \quad (2)$$

As the differential amplifier operates as a subtraction, the collector output of Q3 may also be expressed by the following vector when R1=R2=R3=1 kΩ:

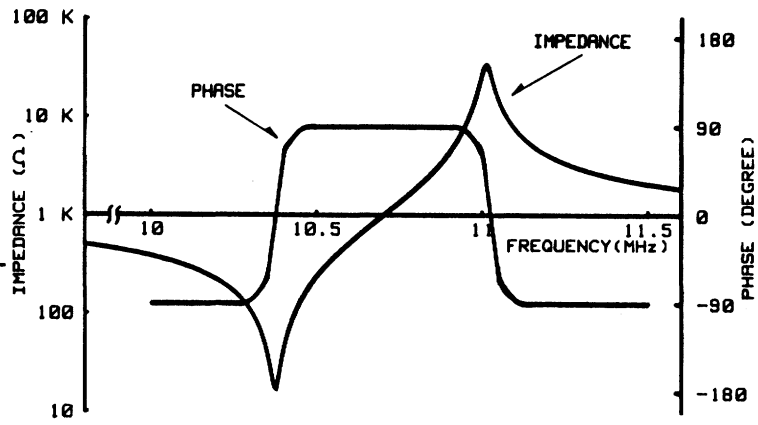


Figure 7: Characteristics of the Ceramic Resonator

$$\vec{V}_{02} = \vec{V}_B - \vec{V}_A$$

$$= \left(V_{IN} \cdot \frac{1-W^2L^2}{2(1+W^2L^2)} , V_{IN} \cdot \frac{-2WL}{2(1+W^2L^2)}\right) \quad (3)$$

As the impedance of the ceramic resonator is 1 kΩ at 10.7 MHz, formula (3) may be expressed by :

$$\vec{V}_{02} = \left(0, V_{IN} \cdot \frac{-1}{2}\right) \quad (4)$$

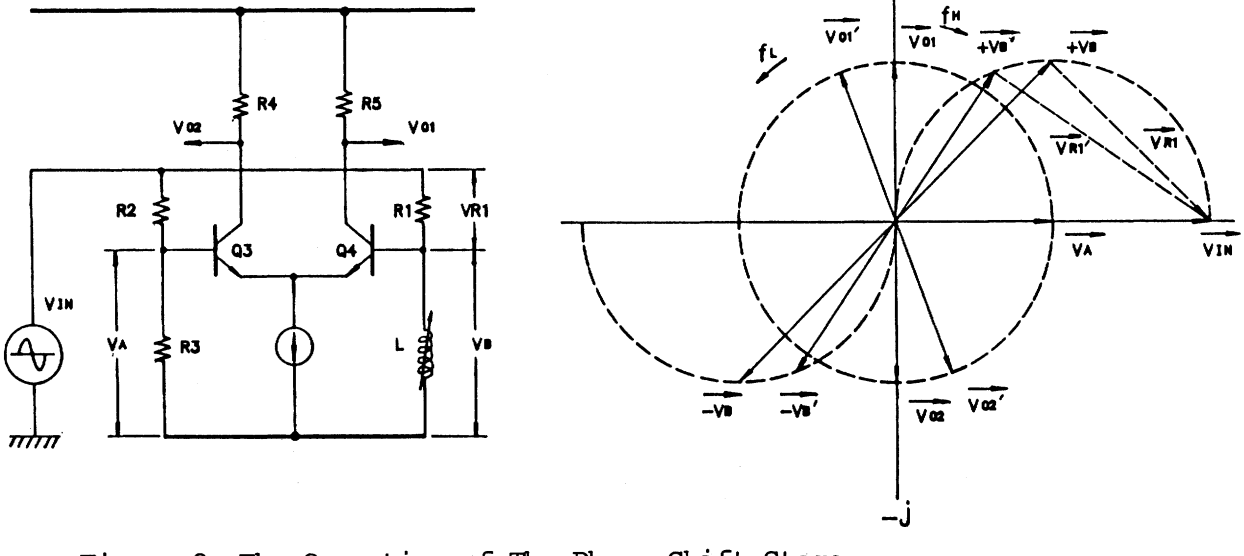


Figure 8: The Operation of The Phase Shift Stage

which is the same as:

$$\vec{V}_{01} = (0, V_{IN} \cdot \frac{1}{2}) \quad (5)$$

Namely, the phase of V_{01} and V_{02} shifts 90 degrees to the V_{IN} at 10.7 MHz. If the IF frequency deviation is higher than 10.7 MHz, the terminal voltage of L rises, and $\vec{V}_{R1}$ shifts to $\vec{V}_{R1}'$. Hence, $\vec{V}_{01}$ shifts to $\vec{V}_{01}'$, and $\vec{V}_{02}$ to $\vec{V}_{02}'$, and V_{01} and V_{02} follow, by the phase deviation interlocking the frequency deviation, a locus of a circle.

The FM is demodulated by inputting the phase-shifted signal and the IF signal into a multiplyer, as shown in Figure 6. As this circuit has a characteristic that enables a constant output amplitude with the frequency deviation, as shown by the locus of the vector in Figure 8, amplitude fluctuation is very small during the frequency deviation to the phase deviation conversion.

Taking a series resonance frequency of f_s and a parallel resonance frequency of f_p,

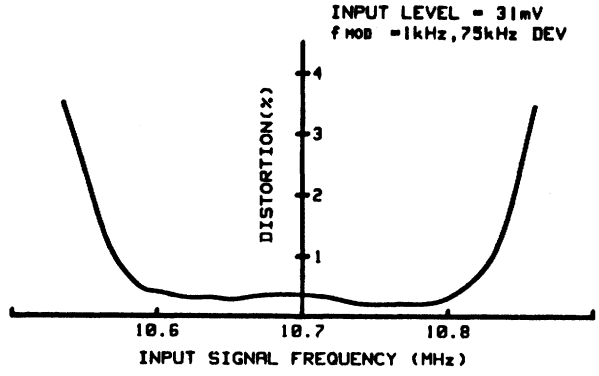


Figure 9: FM IF Distortion to the Input Frequency

the detection gain is:

$$G_V = \frac{\pi}{f_p - f_s} \quad (\text{rad/Hz}) \quad (6)$$

The IF T·H·D is shown in Figure 9.

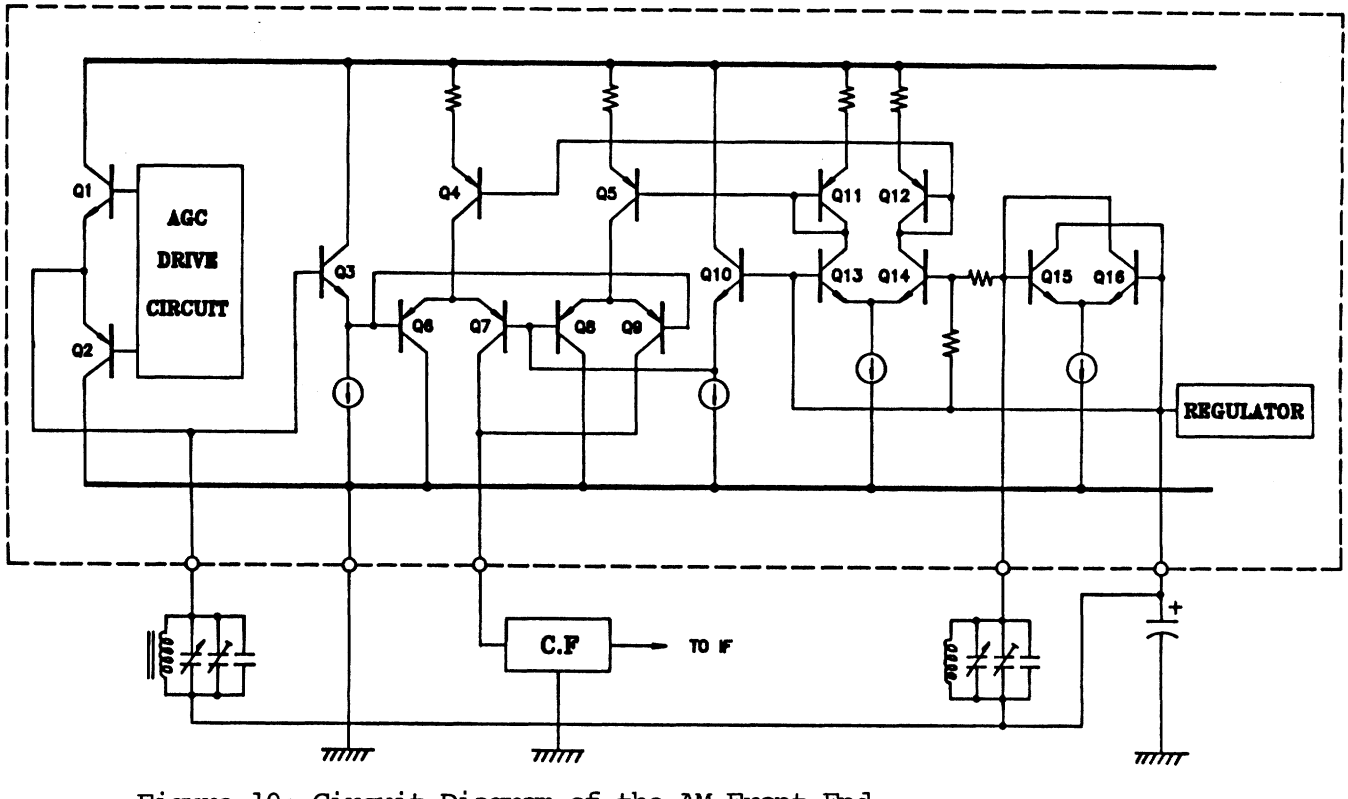


Figure 10: Circuit Diagram of the AM Front End

AM FRONT END

The AM front end consists of a RF amplifier, a local oscillator, a buffer amplifier for the local oscillator, and AGC circuits to control the RF signal level. Figure 10 shows the diagram of the AM front end circuit.

The RF amplifier is a low noise transistor which receives the input signal with the emitter follower.

The mixer is a double-balanced mixer which is constructed by the high performance vertical PNP transistors, Q4 - Q9. Conversion gain is approximately 20 dB.

The local oscillator consists of the differential pair, Q15 and Q16, and is of a positive feedback type. The level of the local oscillator is as low as 600 mVp-p due to the reduction of the leakage to other circuits.

The buffer amplifier, consisting of Q13 and Q14, protects the local oscillator from a large RF input signal, and supplies a differential output of the local oscillator to the double-balanced mixer. The current mirror circuit is constructed by Q11 and Q12 of the buffer amplifier load and Q4 and Q5 of the mixer. Hence mixer current is determined by the current of the buffer amplifier.

The shunt type AGC, Q1 and Q2, reduces the RF input signal with a low impedance against the signal source impedance. The shunt AGC circuits are constructed with symmetrical circuits of NPN and PNP transistors, and make use of the operating base common input impedance from the emitter side in order to eliminate distortion.

The AM front end total gain is approximately 20 dB. NF is 2 dB at a signal source impedance of 25 KΩ. The AM front end is designed to receive a short wave band up to 30 MHz.

AM IF AMPLIFIER AND DETECTOR

The AM IF stage consists of a three-stage differential amplifier, of which the two stages are AGC amplifiers. The third stage has a fixed constant gain of 20 dB, and is controlled by the AGC circuit to maintain an input level of about 80 dBμV, enabling an output of 100 dBμV. The IF amplifiers used are capacitor coupling amplifiers with an effective IF band pass characteristics. The band pass characteristics are shown in Figure 11.

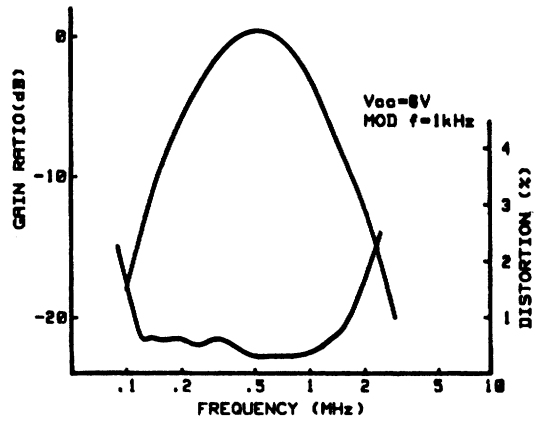


Figure 11: The Band Pass Characteristics of the AM IF Amplifier

A negative feedback rectification circuit is used in the AM detector to enable low distortion and high S/N performance, despite the low input level. Figure 12 shows the equivalent circuit.

The PNP transistors, Q3, Q4, and Q5, are biased to class B by the collector voltage of the differential amplifiers, Q1 and Q2. As a result, half-sine waves are picked up from Q3 and Q4, composed by the current mirror circuits of D3, Q7, and D4, Q8, and then rectified. Q5 and Q6 are negative feedback transistors with a feedback rate of 100 %.

The detection gain may be expressed as follows: First of all, the input current I1 of Q1 to the plus half-wave is:

$$I_1 = \frac{1}{R_I} \cdot e_i(1+m)\sin wt \quad (0 \leq wt \leq \pi) \qquad (7)$$

where m: modulation rate
e_i: signal peak voltage

I_1 also runs through the I_c of the PNP transistor, Q3. The input current I_1' to the minus half-wave is:

$$I_1' = \frac{1}{R_I} \cdot e_i(1+m)\sin wt \quad (\pi \leq wt \leq 2\pi) \qquad (8)$$

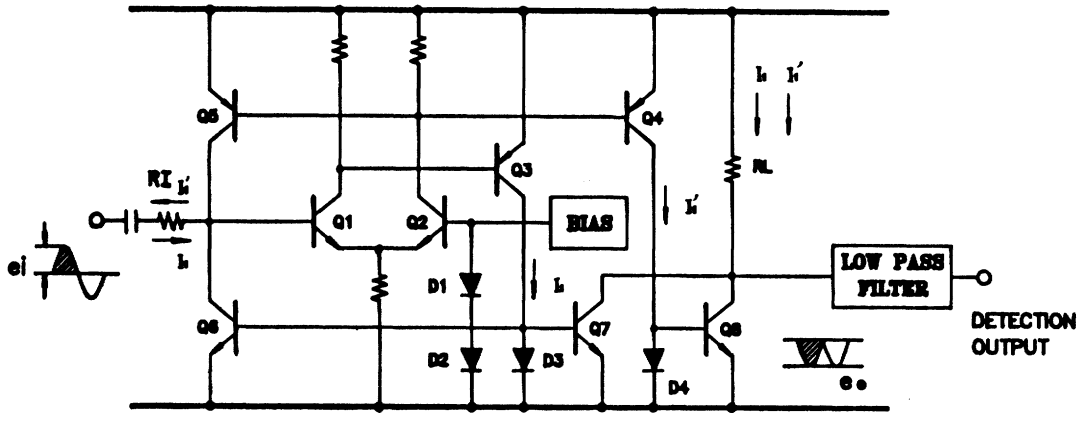


Figure 12: The AM Detector Circuit

I_1' runs through the I_C of the PNP transistors, Q4. From the above, the output voltage e_0 of load R_L is expressed as:

$$e_0 = \frac{R_L}{R_I} \cdot e_i (1+m) \cdot |\sin wt| \qquad (9)$$

e_0 output is given as an absolute value, and detection gain is thus determined by the resistor ratio R_L/R_I. The signal, after passing through the low pass filter in the IC, is expressed as:

$$e_{AF} = \frac{R_L}{R_I} \cdot m \cdot e_i \cdot \frac{2}{\pi} \qquad (10)$$

Figure 13 shows the new circuit in comparison with the conventional diode detector.

AUDIO AMPLIFIER

The audio amplifier includes pre and power amplifiers and an electric volume, and is designed for a low current consumption. The on-chip output stage is made of a complementary single ended push pull using a vertical PNP transistor and a NPN transistor. The Rs of these output transistors is less than 1 Ω, owing to the low series collector resistor structure.

The process of this IC is of a two-level wiring, with the merits of a high packing density and increased freedom of circuit design. We have also found that the efficiency of the power transistor has been remarkably improved, owing to the usage of a second metal pulling out the emitter, which in turn reduces the wiring series resistor for pulling out the emitter compared to the single level wiring, and activate the Emitter-Base junction. And as a result, the area of the power transistor on the chip has been substantially reduced.

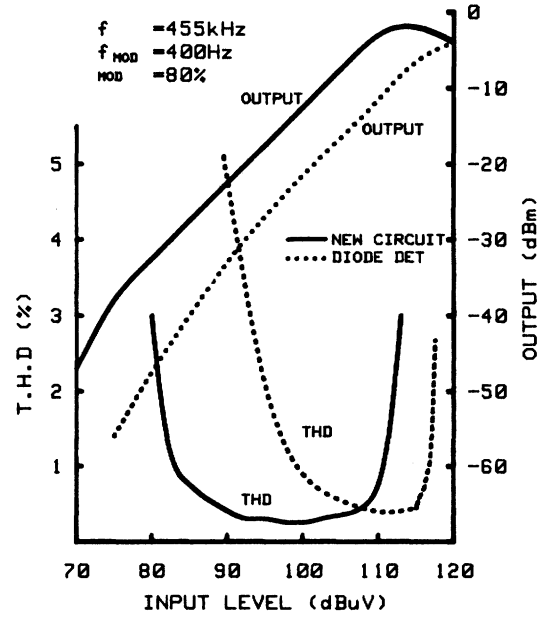


Figure 13: The New Circuit in Comparison with the Conventional Diode Detector

Keeping the collector-emitter saturation voltage of the power transistor low at large currents is essential for obtaining higher efficiency of the power output, restraining the temperature rise in the IC chip, and reducing the thermal effect on the front end circuit.

The saturation voltages of the NPN and PNP transistors are given below:

$V_{CE(SAT)}$ of the NPN transistor

0.5 V TYP (I_C = 1 A, I_B = 50 mA)

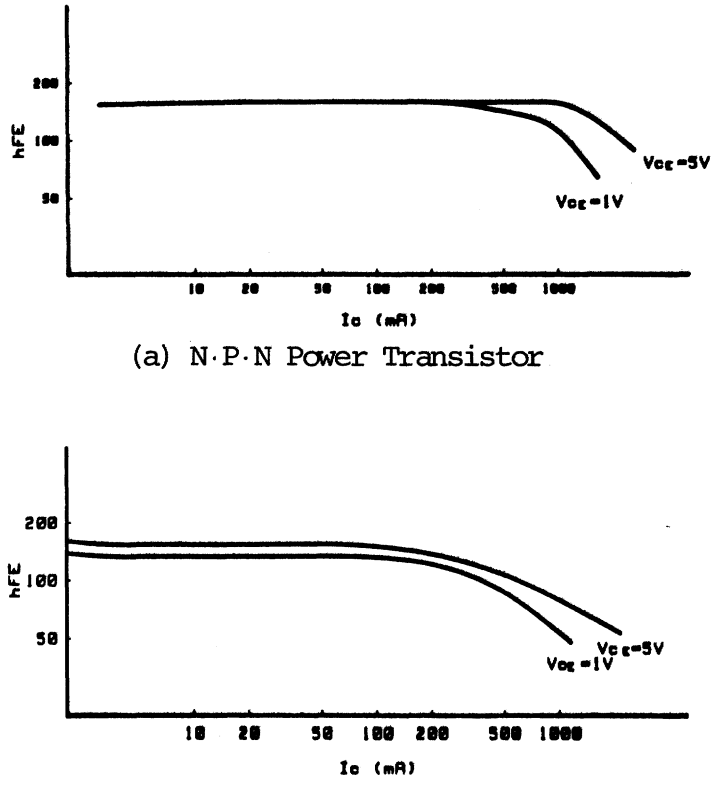
$V_{CE(SAT)}$ of the PNP transistor

0.6 V TYP (I_C = 1 A, I_B = 50 mA)

Figure 14 shows the emitter current gain to the collector current.

The bias current of the final stage is determined by the distortions of cross-over and of switching. Here, a bias current of 800 μA is obtained, owing to an improved linear audio circuit and switching characteristics of the power transistors. The bias current is obtained by a circuit symmetrical to the audio signal path.

Figure 15 shows the circuit diagram of the audio amplifier. These circuits shown in the figure detect and amplify only the signal transformed from the pre amplifier at D4 and D5. Under static condition, the bias current of the output stage is determined by the current of the diode, D4 and D5. For the above reason, the cathode voltage of D5 must be kept accurate, and thus, the circuits of D8, D9, D10, Q10, and Q11 are made symmetrical to the circuits of D4, D5, D6, Q6, and Q8, in order to set a reference voltage. They are then connected to D5 and Q6 through a regulator.



(a) N·P·N Power Transistor

(b) P·N·P Power Transistor

Figure 14: Emitter Current Gain to the Collector Current

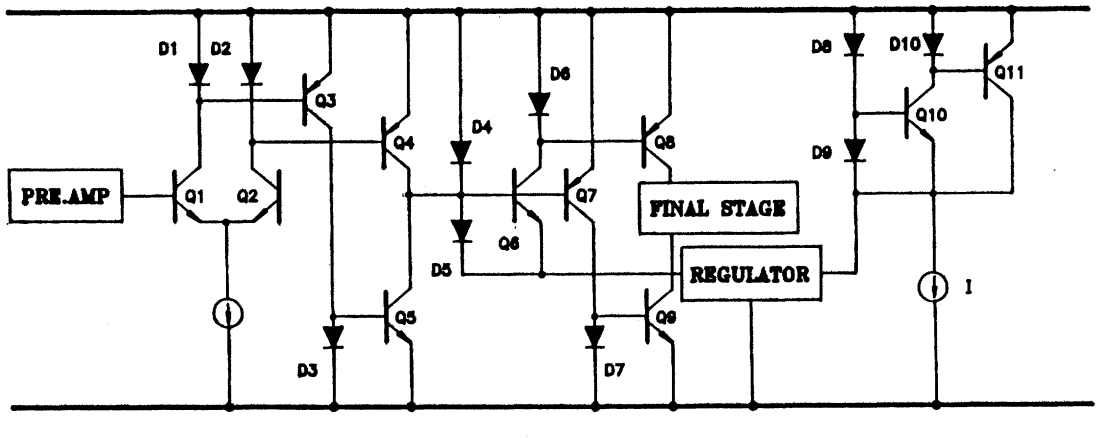


Figure 15: Circuit Diagram of the Power Amplifier

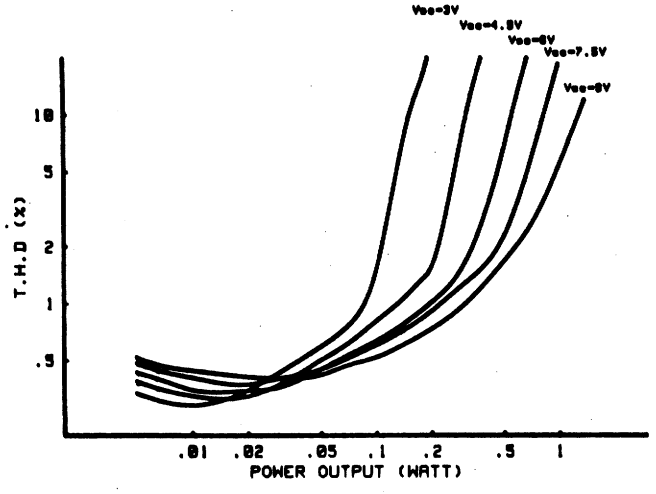


Figure 16: Audio T·H·D to The Power Output

The accuracy of the bias current of the output stage is determined by the current source, and therefore, the current value is stabilized to a large extent. Figure 16 shows the audio T·H·D to the power output.

ELECTRIC VOLUME

Recently, many radio systems are adopting the frequency synthesizer electric tuner. Along with the tuning system, the volume in the IC may also be electrically controlled; the electric volume is constructed with an attenuator in front of the audio pre amplifier input, controlling the gain circuit of the pre amplifier. Here, the volume attenuation is greater than 90 dB.

Figure 17 shows the characteristics of the attenuation. As can be noted from the figure, the attenuation characteristics at the center of the volume curves slowly, enabling easy adjustment of the volume.

REGULATOR

Regulators must be designed by considering the compensation for the local oscillator drift and the thermal stability of each circuit. We have designed a regulator circuit that enables a stable current regardless of the temperature fluctuation.

Figure 18 shows the equivalent circuit. Here, a constant current source I_0 is set which kicks at Q7 to start operating the regulator. I_1 then flows in D3, and due to the close loop consisting of Q7, Q8, D3, Q6, D2, and Q5:

$$I_0 \doteq I_1 \qquad (11)$$

and neither I_1 nor I_0 hold any coefficient. Thus, the coefficient of this regulator output voltage is (resistor plus V_{BE}). Taking into consideration the differential amplifier shown in Figure 18, the circuit connected with the regulator is almost stabilized as well as the current made constant. Figure 19 shows the coefficient of this regulator.

5. Process of the Newly Developed IC

The conditions of the device to accomplish the IC are given as follows:

(1) High f_T
(2) Low noise
(3) Low series collector resistor
(4) Low parasitic capacitor

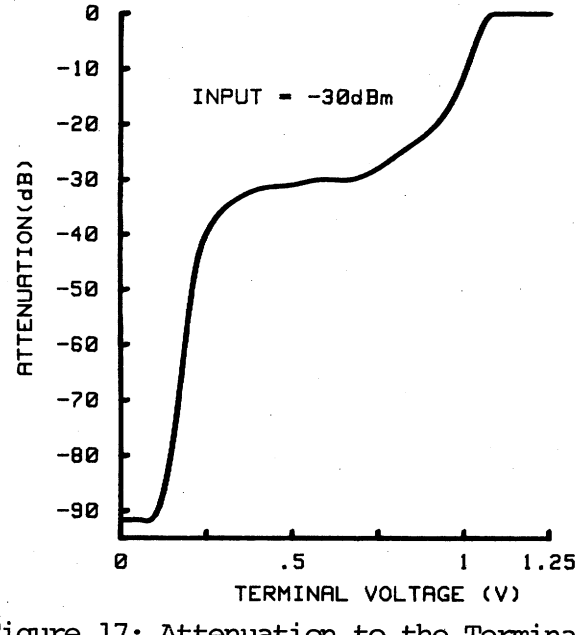


Figure 17: Attenuation to the Terminal Voltage

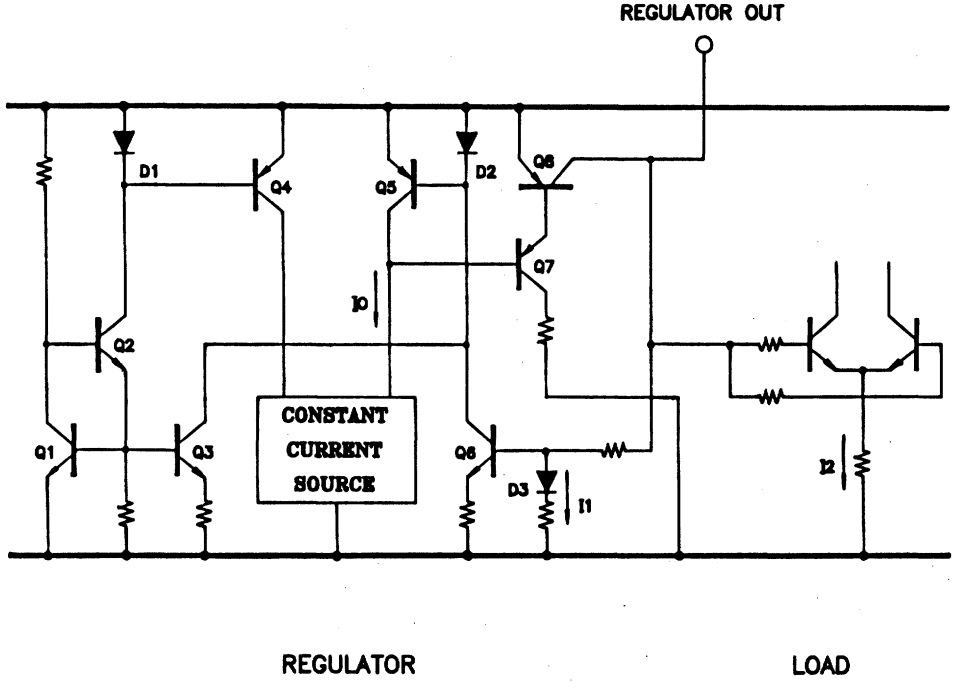


Figure 18: Regulator Circuits

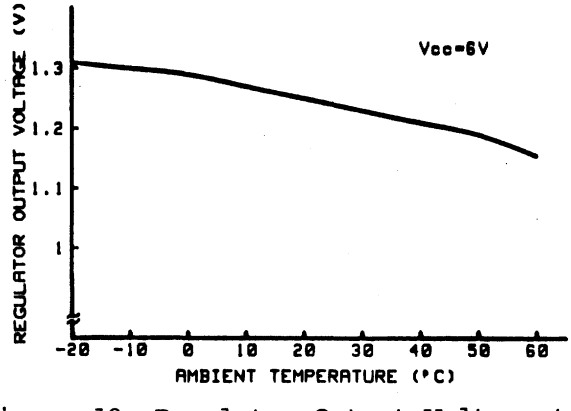


Figure 19: Regulator Output Voltage to the Ambient Temperature

We have developed the new bipolar IC process in the following way to satisfy these conditions:

(a) Employ arsenic for the emitter of the NPN transistor to achieve a high h_{FE} at small currents and a f_T as high as 1.5 GHz.

(b) Implant phosphorus in the base of the vertical PNP, and boron in the emitter, to obtain a f_T of 120 MHz and a h_{FE} of 100∼300.

(c) With bipolar integrated circuits, capacitors can be made either by a P-N junction or a MOS structure. MOS capacitors are preferred in general, but have the drawback of small capacitance values. With this IC, adopt $S_{i_3}N_4$ thin film, where a capacitor of 100 μm x 100 μm would give a capacitance value of 12 PF.

(d) Prepare two different sheet resistivities of 1 KΩ/square and 400Ω/square by ion implantation.

(e) Use a two-level wiring for a higher density and for more freedom of the circuit design.

(f) Use polyimide as the insulator between the two metal layers.

The cross-sectional view of the newly developed IC and a photograph of the IC chip are shown in Figures 20 and 21, respectively.

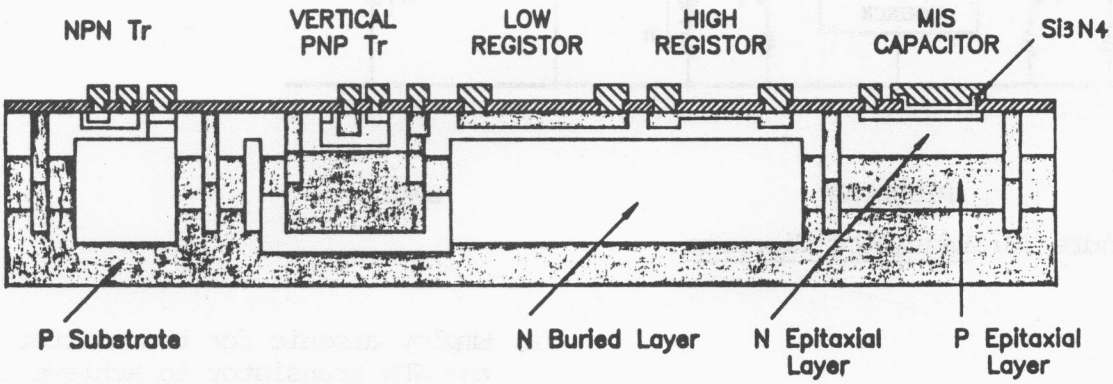


Figure 20: Cross-Sectional View of the Newly Developed IC

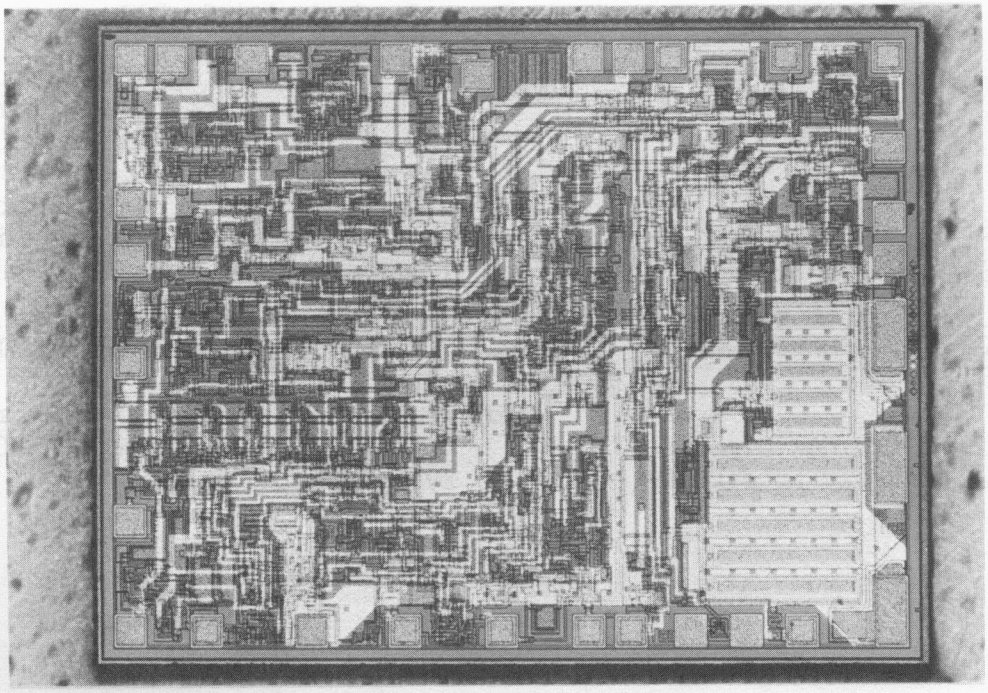
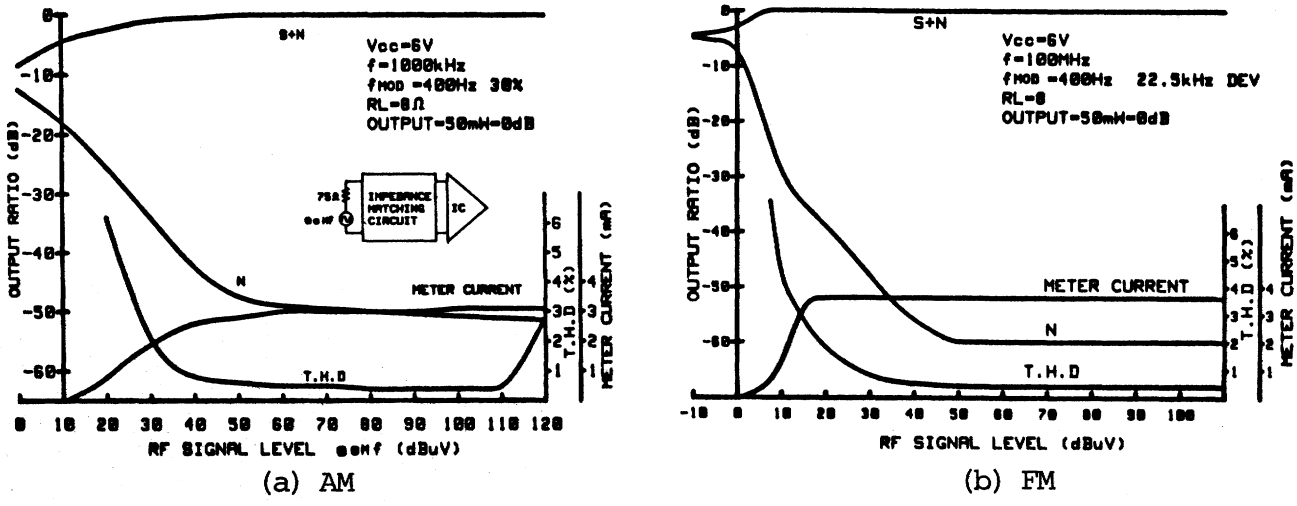


Figure 21: Photograph of the IC



(a) AM (b) FM

Figure 22: The AM/FM S/N Performance

6. Performance of the IC

The summary of the typical characteristics and the AM/FM performance are given in Table 1 and Figure 22, respectively.

(1) Static Characteristics			(3) Dynamic Characteristics – FM MODE f_{FM} =100 MHz f_{MOD} =1 kHz	
* Current Consumption	AM MODE	3.5 mA	* –3dB Limiting Sensitivity	1 uV
	FM MODE	5.2 mA	* S/N (e_{FM}= 10mV, 22.5 KDEV)	60 dB
* Operating Voltage Range		1.8 ~ 9 V	* T.H.D (e_{FM}= 31mV, 75KDEV)	0.3 %
			* 30dB Quieting Sensitivity (22.5 KDEV)	2.5uV
(2) Dynamic Characteristics – AM MODE f_{AM} =1MHz f_{MOD} =1KHz			(4) Dynamic Characteristics–Audio Amplifier Only f= 1KHz R_L = 8Ω	
* S/N 6 dB Sensitivity (75Ω)		0,63 uV	* Power Output (THD = 10 %)	540 mW
* S/N (e_{AM}= 10 mV, 30 % MOD)		50 dB	* T.H.D (P_o = 50 mW)	0.3 %
* T.H.D (e_{AM}= 56 mV, 80 % MOD)		0.6 %		

Table 1: Summary of the Typical Characteristics

7. Application

Figure 23 shows the typical application of the IC. An experimental super micro radio wristwatch incorporating this IC has been developed, and a radio has already been put on the market last fall. A photograph of the super micro radio wristwatch is given in Figure 24.

8. Conclusion

The introduction of this IC into the AM/FM radio has decreased the number of external components to one-fifth of the original, and as the adjustment at the AM/FM detector stage has been completely eliminated, the total adjustment and assembly process have been substantially reduced and simplified. The radio system using this IC enables an extremely high cost-performance and high reliability. This IC is especially useful in the field of battery-operated radios owing to its low power consumption and low voltage operation.

Figure 24: The Experimental Super Micro Radio Wristwatch

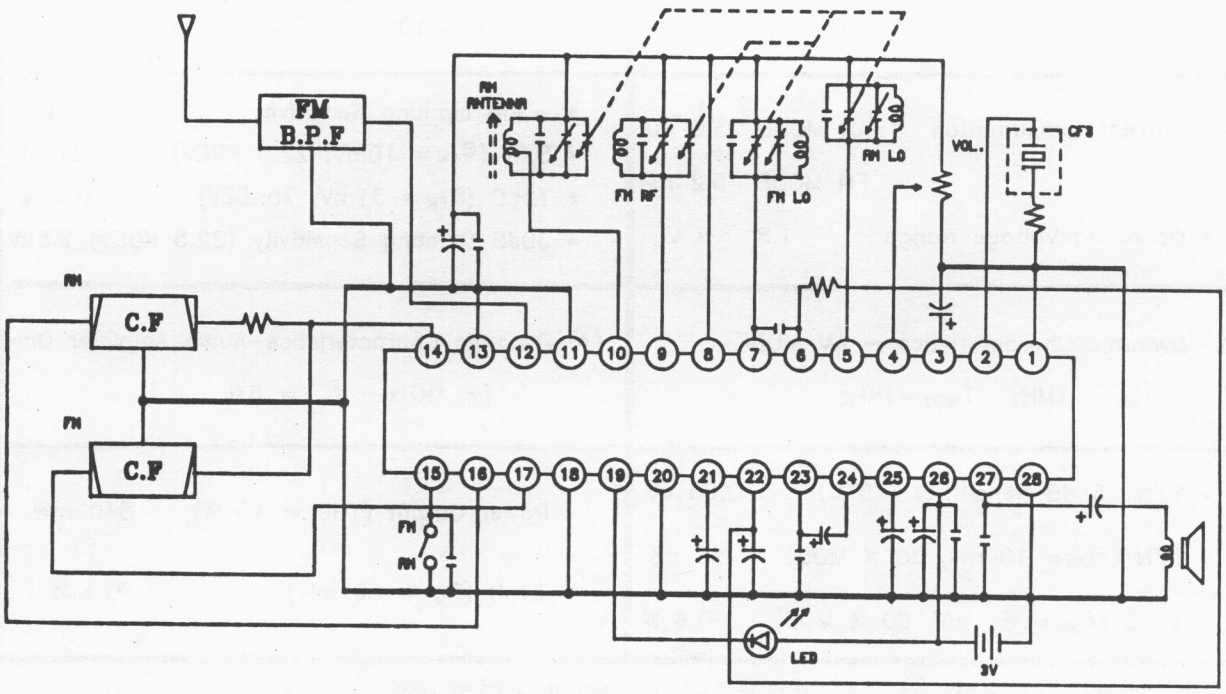


Figure 23: Typical Application of the IC

9. Acknowledgement

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BIOGRAPHY

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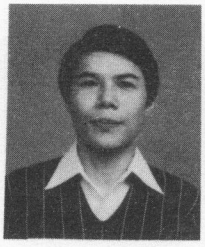

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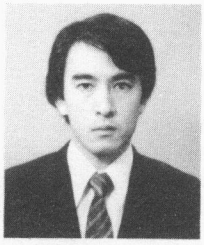

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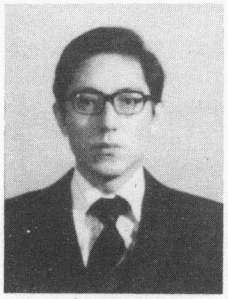

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