BEE 233 Circuits Fall 2015
Lab 2: RC circuits

1 Objectives

1. Measure the output waveform of simple RC circuits excited by step functions.
2. Calculate and measure various timing parameters, including the time constant, rise and fall times and the propagation delays.
3. Compare expected and experimentally measured values.

2 First and second order RC circuits

These are the circuits you'll be experimenting with in this lab in figures 1 and 2.

The first order circuit in figure 1 is called that because it contains only one energy storage component, i.e., one capacitor.

The second order circuit in figure 2 contains two energy storage components, i.e., two capacitors.

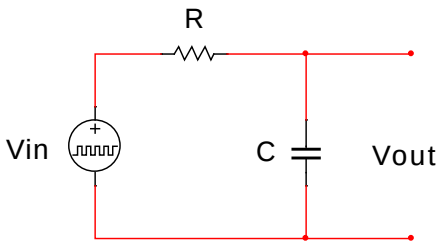


Figure 1. First order RC circuit.

3 First order RC circuit

3.1 Step response and timing parameters

Figures 3 and 4 illustrate the step response of a first-order RC circuit. With only a single capacitor, the response is an exponential signal with a time constant, $\tau = RC$.

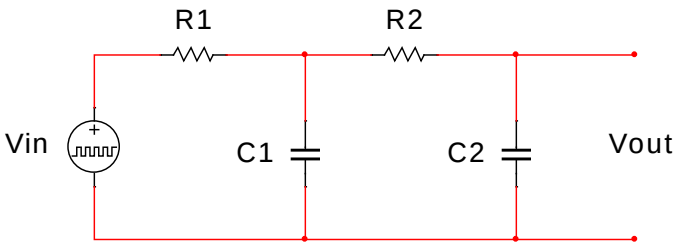


Figure 2. Second order RC circuit.

Four other timing parameters are important in describing how fast or slow an RC circuit responds to a step input. We measure them separately for rising and falling edges.

Rising edge

Parameter	*Definition*
$t_{10\%(rising)}$	Time to reach Vout = 10% of maximum.
t_{PLH} = $t_{50\%(rising)}$	The propagation time from low to high, defined as the time from the 50% point on Vin to the 50% point on Vout.
$t_{90\%(rising)}$	Time to reach Vout = 90% of maximum.
t_{RISE}	The rise time, defined as $t_{90\%(rising)} - t_{10\%(rising)}$

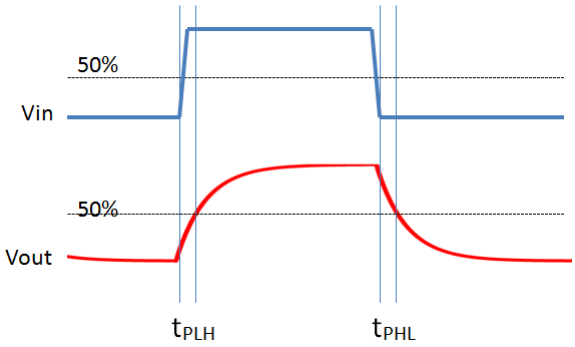


Figure 3. t_{PLH} and t_{PHL} are measured from input to output.

Falling edge

Parameter	*Definition*
$t_{90\%(falling)}$	Time to reach Vout = 90% of maximum.
t_{PHL} = $t_{50\%(falling)}$	The propagation time from high to low, defined as the time from the 50% point on Vin to the 50% point on Vout.
$t_{10\%(falling)}$	Time to reach Vout = 10% of maximum.
t_{FALL}	The fall time, defined as $t_{10\%(falling)} - t_{90\%(falling)}$

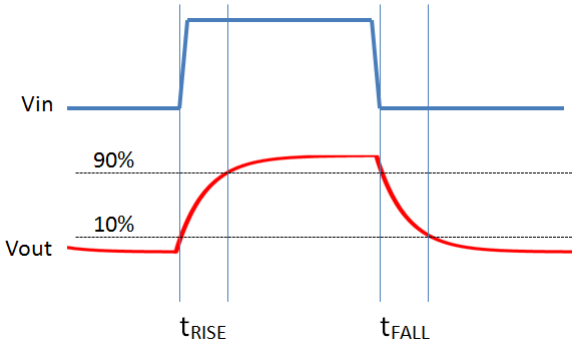


Figure 4. t_{RISE} and t_{FALL} are are measured between the 10% and 90% points on the output.

The rising and falling times are measured between different points on the same Vout curve. But the rest of the parameters are measured between rising or falling edge on Vin and Vout achieving the specified percentage of the maximum value.

3.2 Parameter extraction

The important parameters of Vout are the maximum amplitude and the time constant τ. The maximum amplitude is easily measured using the oscilloscope. To measure the time constant directly and accurately is more difficult since the waveform is an exponential function of time.

The log of an exponential function is linear. If Vout is an exponential function of time, then *log*(Vout) will be a linear function of time. Starting with the equation for Vout during the period it falls, it's possible to derive a new function *log*(Vout) that is linear in terms of the time t. The slope of this line is then used to extract the time constant τ.

Alternatively, the calculation can be done starting with the equation for Vout during the time it rises. When rising, *log*(1-Vout/A) is linear in time and can also be used to extract the time constant.

In the lab, you will measure a set of data points (t, Vout). These values, after manipulating in this manner, can be used to plot a straight line, whose slope, τ, can be extracted using a least squares fit with tools like Excel.

3.3 Delay models

RC circuits are frequently used to model the timing characteristics of computer systems. When one logic gate drives another gate, the input circuit of the second gate can be modeled as an RC load. The propagation delay through the first gate can then be calculated assuming ideal square wave input and the RC load. The longer the delay time, the slower the circuit can be switched and the slower the computer is. Conversely, the shorter the delay time, the faster the computer is. This delay time is called "gate delay" since it relates to driving characteristics of a logic gate.

Another use of RC circuits is to model wiring characteristics of bus lines on integrated circuits (IC) or on printer-circuit boards (PCB). A wire can be modeled as many cascaded sections of simple RC circuits. When a square wave is applied to one end of the bus, it takes time for the signal to propagate to the other end. This delay time due to the wire can be calculated based on the values of R and C in each section and the number of sections used to model the wire. The longer the wire, the more sections are needed for accurate model. A wire is also referred to as "interconnect" and the delay due to a wire is also called "interconnect delay." In high-frequency systems, the interconnect delay tends to dominate the gate delay and is a fundamental constraint on how fast a computer can operate.

3.4 Equations for the first order circuit

Assume the input signal, Vin, to the circuit in Figure 5 (same as figure 1) is a perfect square wave with amplitude A (from 0 V to A), and a period T where $T \gg RC$. Using only symbolic parameters, no numerical values, derive equations for the following. With ideal components, rising and falling times will be exactly symmetric.

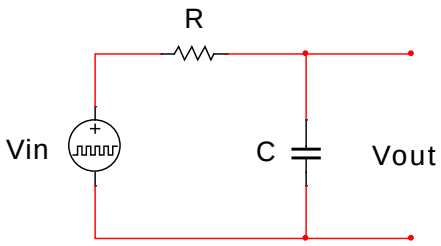


Figure 5. First order RC circuit.

1. Vout(t) when rising and when falling and the maximum and minimum values.
2. $t_{10\%}$, t_{PLH} and $t_{PHL} = t_{50\%}$ and $t_{90\%}$, rising and falling.

3. $t_{RISE} = t_{FALL}$.

3.5 Equations for parameter extraction

From the equations for Vout(t) for the circuit in Figure 5:

1. Derive an equation for either *log*(Vout(t)) when falling or *log*(1-Vout/A) when rising. Either of these equations should be linear in terms of t.
2. From that, derive an equation for the slope of this line in terms of the time constant τ.

3.6 Experimental procedures

1. Build the circuit in Figure 5 using the following component values. Measure your resistor.

   R = 10 KΩ
   C = 0.01 μF
   Vin = 3.0 Vpp square wave at 300 Hz with DC offset = 1.5 V

   The input frequency has been chosen to ensure that T ≫ RC, where T = 1/f. This guarantees that Vout has sufficient time to reach a final value before the next input transition.

2. Capture the following screenshots. Vin should be on channel 1 and Vout on channel 2. *Use DC coupling.*
   a. Vin and Vout with on-screen measurements of frequency, Vpp for Vin and Vout, and cursors positioned to measure the pulse width for Vin.
   b. Same as (a), but with cursors repositioned to measure each of the following, one measurement per screenshot.
      i. t_{PLH}
      ii. t_{PHL}
      iii. t_{RISE}
      iv. t_{FALL}
3. Record measurements of $t_{10\%}$ and $t_{90\%}$ rising and falling.
4. Record at least 10 measurements of Vout versus time during either the rising or falling interval, where time is measured from the rising or falling edge on the input.

3.7 Data analysis

1. Create a table comparing expected versus measured values for rising and falling values of $t_{10\%}$, t_{PLH} and $t_{PHL} = t_{50\%}$, and $t_{90\%}$, and also for t_{RISE} and t_{FALL}. Explain any

differences. Is it important to consider the internal source resistance of the function generator?

2. Create a table of the 10 data points collected in section 7.1.4 and add a third column where you've applied the logarithmic function discussed in section 6.2, namely log(Vout) falling or log(1 – Vout/A) rising, to your measurements of Vout. Plot any 5 of these 10 transformed data points versus time and use the best-fit technique to extract the slope of the line and from that, the time constant τ. Compare this value with the expected value RC and compute the difference in percent.
3. Plot all 10 transformed data points and repeat the best-fit technique to extract the time constant once again. Compare this value to the value computed using only 5 points.
4. Assuming that this new value for τ is the more accurate, use it to compute the correct value of the capacitor C. Compare the computed value of the capacitor with the marked value.

4 Second order circuit

4.1 Simulation of the second order circuit

1. Create a Multisim or SPICE simulation of the second order circuit in figure 6 (same as figure 2) using the following values and capture an image of the schematic. (To copy a schematic from Multisim into Word, start in Multisim by selecting and copying all (Ctrl-A, Ctrl-C). Then in Word, "Paste Special" as a "Picture (Enhanced Metafile)".)

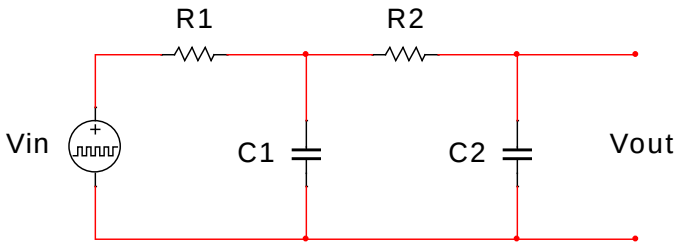
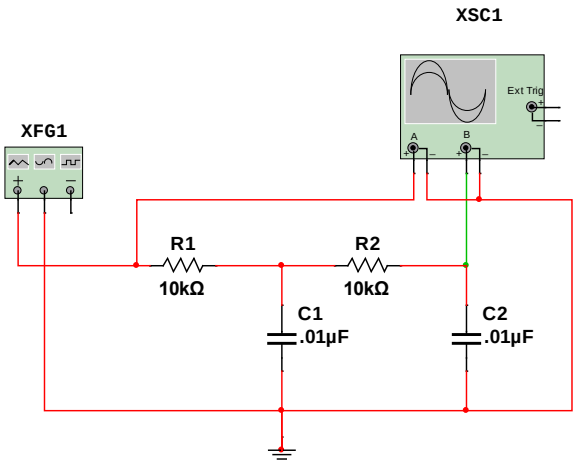
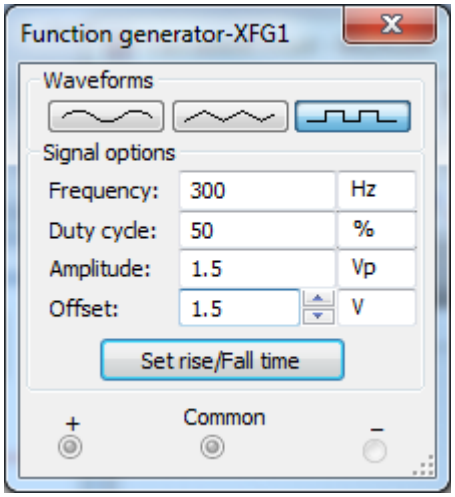


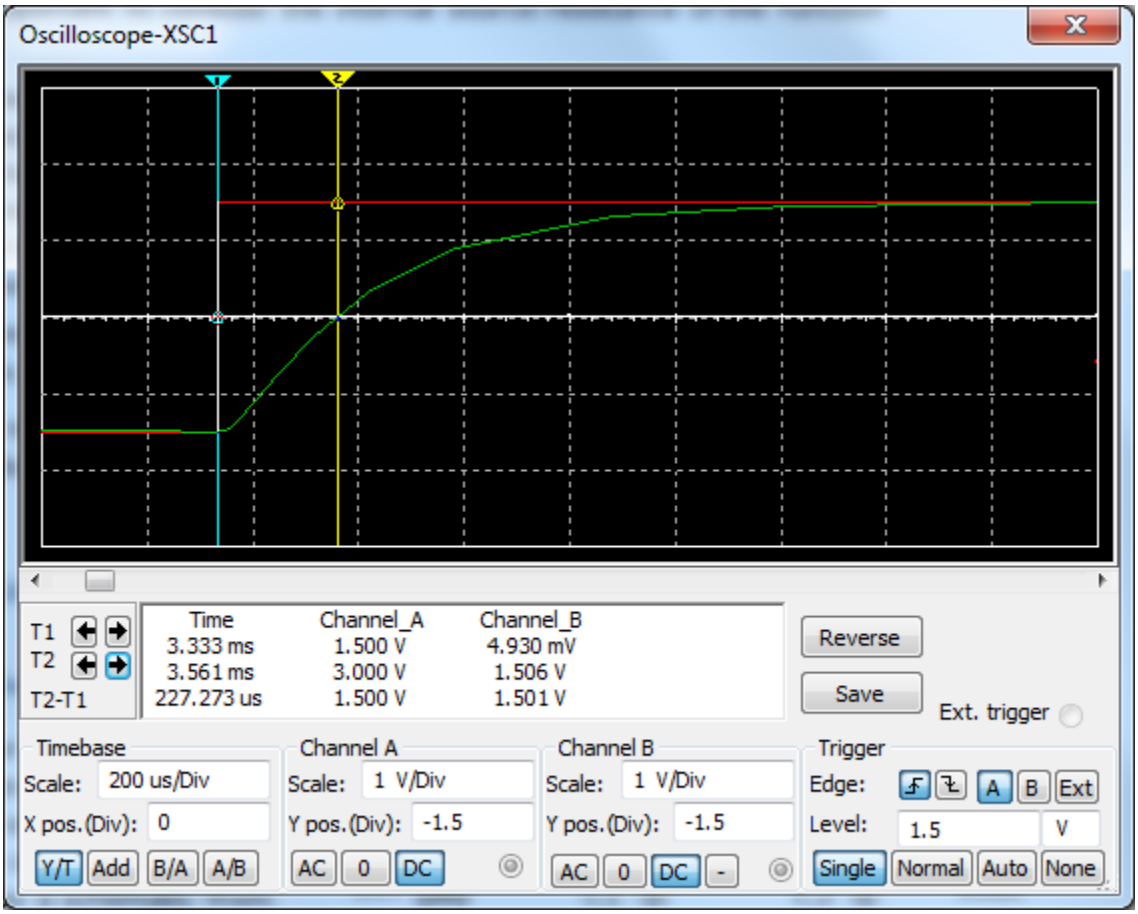
Figure 6. Second order RC circuit.

R1 = R2 = 10 KΩ
C1 = C2 = 0.01 μF
Vin = 3.0 Vpp square wave at 300 Hz with DC offset = 1.5 V

Here's an example from my own simulation, showing the function generator settings and a screenshot of my own measurement of t_{PLH}. (You will do t_{PHL}.) Notice how LARGE I've made it so it can be read with ease.







2. Use the simulation to determine the expected values of t_{PHL}. Capture a screenshot.

4.2 Experimental procedures

1. Build the circuit in Figure 6 using the following component values. Measure your resistors.

   R1 = R2 = 10 KΩ
   C1 = C2 = 0.01 μF
   Vin = 3.0 Vpp square wave at 300 Hz with DC offset = 1.5 V

2. Capture the following screenshots. Vin should be on channel 1 and Vout on channel 2. *Use DC coupling.*

   a. Vin and Vout with on-screen measurements of frequency, Vpp for Vin and Vout, and cursors positioned to measure the pulse width for Vin.

   b. Same as (a), but with cursors repositioned to measure t_{PLH} and again for t_{PHL}.

4.3 Analysis

1. Compare the simulated and measured values for the second order circuit.
2. Compare the t_{PLH} and t_{PHL} delay times for the simple, first order circuit with those for the cascaded second order circuit.
3. Is the delay twice as large for two stages as it for one? Do the delay times scale with the number of sections? Explain.